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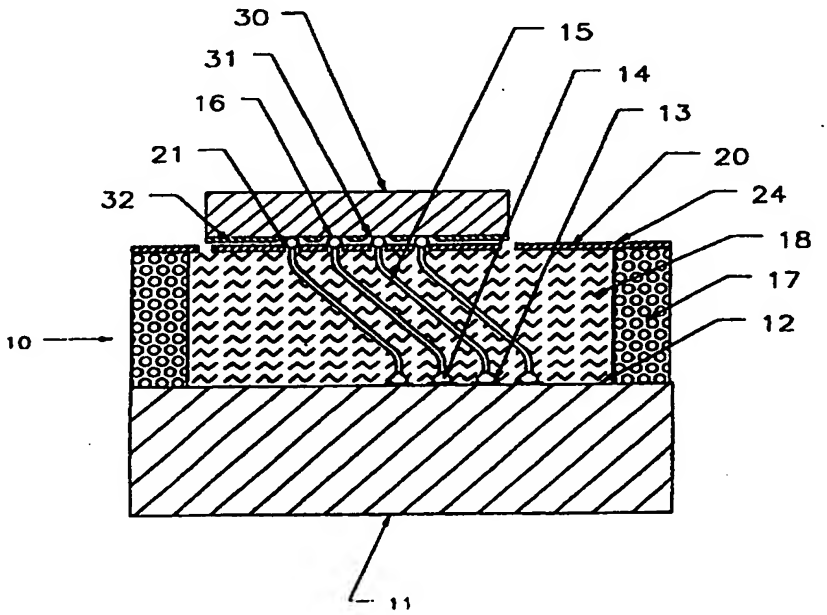

(57) Abstract

The present invention is directed to a structure comprising a substrate having a surface; a plurality of elongated electrical conductors extending away from the surface; each of said elongated electrical conductors having a first end affixed to the surface and a second end projecting away from the surface; there being a plurality of second ends; and a means for maintaining the plurality of the second ends in substantially fixed positions with respect to each other. The structure is useful as a probe for testing and burning in integrated circuit chips at the wafer level.

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INTEGRATED COMPLIANT PROBE FOR WAFER LEVEL TEST AND BURNIN

This application claims priority from Provisional Application U.S. Serial No. 60/026,112 which was filed on September 13, 1996.

CROSS REFERENCE TO RELATED APPLICATION

The teaching of U.S. Application Serial No. _____ filed on the same day herewith entitled, "WAFER SCALE HIGH DENSITY PROBE ASSEMBLY, APPARATUS FOR USE THEREOF AND METHODS OF FABRICATION THEREOF" to Brian S. Beaman et al. and the teaching of U.S. Application Serial No. _____ filed on the same day herewith entitled, "PROBE STRUCTURE HAVING A PLURALITY OF DISCRETE INSULATED PROBE TIPS PROJECTING FROM A SUPPORT SURFACE, APPARATUS FOR USE THEREOF AND METHODS OF FABRICATION THEREOF" to Brian S. Beaman et al. is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention is directed to structures, methods of fabrication and apparatus for use thereof for testing of electronic devices, such as integrated circuit devices and other electronic components and particularly to testing of integrated circuit devices with rigid interconnection pads and multi-chip module packages with high density interconnection pads.

BACKGROUND OF THE INVENTION

Integrated circuit (IC) devices and other electronic components are normally tested to verify the electrical function of the device and certain devices require high temperature burn-in testing to accelerate early life failures of these devices. Wafer probing is typically done on a single chip site at temperatures ranging from 25C - 125C while burn-in is typically done on diced and packaged chips at temperatures ranging from 80C to 150C. Wafer probing and IC chip burn-in at elevated temperatures of up to 200C has several advantages and is becoming increasingly important in the semiconductor industry. Simultaneous testing of multiple chips on a single wafer has obvious advantages for reducing costs and increasing production throughput and is a logical step towards testing and burn-in of an entire wafer.

The various types of interconnection methods used to test these devices include permanent, semi-permanent, and temporary attachment techniques. The permanent and semi-permanent techniques that are typically used include soldering and wire bonding to provide a connection from the IC device to a substrate with fan out wiring or a metal lead frame package. The temporary attachment techniques include rigid and flexible probes that are used to connect the IC device to a substrate with fan out wiring or directly to the test equipment.

The permanent attachment techniques used for testing integrated circuit devices such as wire bonding to a leadframe of a plastic leaded chip carrier are typically used for devices that have low number of interconnections and the plastic leaded chip carrier package is relatively inexpensive. The device is tested through the wire bonds and leads of the plastic leaded chip carrier

and plugged into a test socket. If the integrated circuit device is defective, the device and the plastic leaded chip carrier are discarded.

The semi-permanent attachment techniques used for testing integrated circuit devices such as solder ball attachment to a ceramic or plastic pin grid array package are typically used for devices that have high number of interconnections and the pin grid array package is relatively expensive. The device is tested through the solder balls and the internal fan out wiring and pins of the pin grid array package that is plugged into a test socket. If the integrated circuit device is defective, the device can be removed from the pin grid array package by heating the solder balls to their melting point. The processing cost of heating and removing the chip is offset by the cost saving of reusing the pin grid array package.

The most cost effective techniques for testing and burn-in of integrated circuit devices provide a direct interconnection between the pads on the device to a probe sockets that is hard wired to the test equipment. Contemporary probes for testing integrated circuits are expensive to fabricate and are easily damaged. The individual probes are typically attached to a ring shaped printed circuit board and support cantilevered metal wires extending towards the center of the opening in the circuit board. Each probe wire must be aligned to a contact location on the integrated circuit device to be tested. The probe wires are generally fragile and easily deformed or damaged. This type of probe fixture is typically used for testing integrated circuit devices that have contacts along the perimeter of the device. This type of probe is also much larger than the IC device that is being tested and the use of this type of probe for high temperature testing is limited by the probe structure and material set. This is described with reference to applicant's co-pending U.S. Application Serial No. 08/754,869

filed on November 22, 1996.

Another technique used for testing IC devices comprises a thin flex circuit with metal bumps and fan out wiring. The bumps are typically formed by photolithographic processes and provide a raised contact for the probe assembly. The bumps are used to contact the flat or recessed aluminum bond pads on the IC device. An elastomer pad is typically used between the back of the flex circuit and a pressure plate or rigid circuit board to provide compliance for the probe interface. This type of probe is limited to flexible film substrate materials that typically have one or two wiring layers. Also, this type of probe does not provide a wiping contact interface to ensure a low resistance connection.

The aluminum bond pads on a high density IC device are typically rectangular in shape and are recessed slightly below the surface of the passivation layer. If the wiping action of the high density probe is not controlled, the probe contact may move in the wrong direction and short to an adjacent aluminum bond pad or the probe contact may move off of the aluminum bond pad onto the surface of the passivation layer and cause an open connection.

Gold plated contacts are commonly used for testing and burn-in of IC devices. The high temperature test environment can cause diffusion of the base metal of the probe into the gold plating on the surface. The diffusion process creates a high resistive oxide layer on the surface of the probe contact and reduces the probe life.

The position of the probe tips must be controlled to ensure accurate alignment of the probes to the interconnection pads on the IC device.

During high temperature burn-in testing, the thermal expansion mismatch between the probe structure and the IC device is preferably small to ensure that the probe position does not vary significantly over the burn-in temperature range. Thermal expansion mismatch within the probe structure can result in contact reliability problems.

The challenges of probing a single high density integrated circuit device are further multiplied for multi-chip and full wafer testing applications. Probe fabrication techniques and material selection are critical to the thermal expansion and contact alignment considerations. A small difference in the thermal expansion of the substrate, wafer, and probe construction will cause misalignment of the probe tip to the wafer contact pad. Compliance of the probe structure is another critical factor. Slight variations in the wafer metallization, warpage of the wafer, and slight variations in the probe height contribute to the total compliance requirements for the probe structure.

The prior art described below includes a several different probe fixtures for testing bare IC chips.

U.S. patent 5,177,439, issued January 5, 1993 to Liu et al. is directed to fixtures for testing bare IC chips. The fixture is manufactured from a silicon wafer or other substrate that is compatible with semiconductor processing. The substrate is chemically etched to produce a plurality of protrusions to match the I/O pattern on the bare IC chip. The protrusions are coated with a conductive material and connected to discrete conductive fanout wiring paths to allow connection to an external test system. The probe geometry described in this patent does not provide a compliant interface for testing the aluminum bond pads on the IC device and does not provide a wiping contact interface. The substrate used for fabrication of this probe fixture is

limited to semiconductor wafers which are relatively expensive.

Applicant's co-pending U.S. Application Serial No. 08/754,869, filed on November 22, 1996, the teaching of which is incorporated herein by reference, describes a high density test probe for integrated circuit devices. The probe structure described therein uses short metal wires that are bonded on one end to the fanout wiring on a rigid substrate. The wires are preferably encased in a compliant polymer material to allow the probes to compress under pressure against the integrated circuit device. The wire probes are sufficiently long and formed at an angle to prevent permanent deformation during compression against the integrated circuit device.

OBJECTS

It is the object of the present invention to provide a probe for testing electronic devices and other electronic components that use bond pads for the interconnection means.

Another object of the present invention is to provide a probe structure that is an integral part of the fan out wiring on the test substrate or other printed wiring means to minimize the electrical conductor length as well as the contact resistance of the probe interface.

A further object of the present invention is to provide a probe with a compliant interface to compensate for slight variations in the rigid bond pad heights on the IC device and variations in the height of the probe contacts.

An additional object of the present invention is to provide a raised probe tip for contacting recessed surfaces on the IC device.

Yet another object of the present invention is to provide a probe with a wiping contact interface where the direction and length of the contact wipe is controllable.

Yet a further object of the present invention is to provide a probe construction that has thermal expansion characteristics that are matched to the IC device to be tested or burned-in at high temperature.

Yet an additional object of the present invention is to provide a probe construction that has high durability and reliability for repeated thermal and mechanical cycling.

Yet another object of the present invention is to provide a probe structure that can be used for single chip or multiple chip wafer testing.

Yet another object of the present invention is to provide a probe structure that has an improved true position tolerance.

Yet another object of the present invention is to provide a probe structure that does not require an elastomer material to support the individual probe wires.

It is another object of the present invention to provide a high density probe with controlled wipe can be fabricated on a variety of inexpensive substrate with the fanout wiring.

SUMMARY OF THE INVENTION

A broad aspect of the present invention is a structure comprising a

substrate having a surface; a plurality of elongated electrical conductors extending away from the surface;
each of said elongated electrical conductors having a first end affixed to the surface and a second end projecting away from the surface; there being a plurality of second ends; and a means for maintaining the plurality of the second ends in substantially fixed positions with respect to each other.

In a more particular aspect of the present invention in the structure is useful as a probe to test and burn-in integrated circuits, in particular at the water level.

In another more particular aspect of the present invention the probe is incorporated onto a test apparatus.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features, and advantages of the present invention will become apparent upon further consideration of the following detailed description of the invention when read in conjunction with the drawing figures, in which:

FIGURE 1 shows a cross section of a preferred embodiment of the compliant test probe attached to a substrate and pressed against the aluminum bond pads, such as aluminum pads, on an integrated circuit device.

FIGURE 2 shows a magnified cross section of a preferred embodiment of the compliant test probe.

FIGURES 3-5 show the processes used to fabricate the compliant test probe on a fan out wiring substrate.

FIGURE 6 shows a cross section of a preferred embodiment of the compliant test probe array for testing multiple IC devices on a single wafer.

FIGURE 7 shows a top view of a compliant test probe array for testing all of the IC devices on a single wafer.

FIGURE 8 shows a cross section of a first alternate embodiment of the compliant test probe.

FIGURE 9 shows a magnified cross section of a first alternate embodiment of the compliant test probe.

FIGURE 10 shows a cross section of a second alternate embodiment of the compliant test probe.

FIGURE 11 shows a cross section of a third alternate embodiment of the compliant test probe.

FIGURE 12 shows a cross section of a fourth alternate embodiment of the compliant test probe.

FIGURE 13 shows a cross section of a fifth alternate embodiment of the compliant test probe array for testing multiple IC devices on a single wafer.

FIGURE 14 shows a top view of a fifth alternate embodiment of the compliant test probe array for testing all of the IC devices on a single

substrate.

FIGURE 15 schematically shares a variety of shapes of probe wires useful to practice the present invention, such as "S" showed "C" shaped, continuously curved, piece wire curved, piece wire linear and combinations thereof.

FIGURE 16 schematically shows alternative embodiments of compliant frame structures (17) to support probe tip positioning structure (20) to be maintaining in position and to move as the probe tip ends (16) move when they are moved into engagement with electronic device pads (31).

Figure 17 schematically shows elongated conductors having coatings over the entire conductor or at least at the ends.

FIGURE 18 schematically shows an apparatus for moving the probes according to the present invention into an out of electrical engagement with a workpiece, such as on an integrated circuit (IC), being tested.

DETAILED DESCRIPTION

FIGURE 1 shows a cross section of a test substrate (11) and a compliant test probe (10) according to the present invention. The test substrate (11) provides a rigid base for attachment of the probes (10) and fan out wiring from the high density array of probe contacts to a larger grid of pins or other interconnection means to the equipment used to electrically test the integrated circuit device. The fan out substrate can be made from various materials and constructions including single and multi-layer ceramic with thick or thin film wiring, silicon wafer with thin film wiring, or epoxy glass

laminate construction with high density copper wiring. The test probes (10) are attached to the first surface (12) of the substrate (11). The probes are used to contact the bond pads (31), typically fabricated from aluminum, on the integrated circuit device (30). The bond pads (31) are typically recessed slightly below the surface of the passivation layer (32) of the integrated circuit device (30). The geometry of the compliant test probe (10) is optimized to provide a wiping contact interface to penetrate the oxides on the surface of the aluminum bond pads (31) to provide a low resistance connection. The substrate (11) can be a circuitized substrate typically used to provide a packaging substrate to mount an integrated circuit thereon, such packaging substrates are typically metallized ceramic and glass ceramic substrates and metallized polymer substrates usually referred to as printed circuit boards.

The test probe (10) is attached directly to the fan out wiring (13) on the first surface (12) of the substrate (11) to minimize the resistance of the probe interface. This can be achieved by building test probe (10) on surface (12) or by separately building substrate (10) separately and thereafter attaching it to surface (12) such as by adhesive bonding. The probe geometry is optimized to provide a flexible contact interface that controls the direction and length of the wiping action. Flexibility is provided preferably by using an elastomeric material to fabricate probe (W). However, any other means of providing compliance can be used, such as by a mechanical construction. The elastomer material (18) surrounding the probes provides an compliant structure and the sheet (20) is used to control the position of the probe tips (16). Sheet (20) is typically thin (preferably less than 10 mills) and made of a rigid material such as a metal copper, aluminum, Invar, molybdenum and Cu/Invar/Cu, but can be a polymer sheet such as a polyimide or inorganic sheet such as a ceramic or silicon or glass or a dielectric material

sheet. The sheet is most preferably Invar. The thin Invar sheet (20) is coated with an thin layer of material (24) to insulate the Invar sheet (20) from the probe wire (15) and tip (16). The true position tolerance of the probe tips (16) is enhanced by using a plurality of small holes (21) in the thin Invar sheet (20). The diameter of the holes (21) in the thin Invar sheet (20) are preferably only slightly larger than the diameter of the probe wire (15) and the holes (21) are preferably created using a precision chemical etching process. The diameter (d) of holes (21) as compared to the diameter (r) of area (15) determines the extent to which the tips (16) move away from an initial position as the probe (10) is pressed against a work piece to be tested. Probe tips (16) are typically designed to be aligned with the center of the pad to be probed. The probe tip (16) can move laterally by a distance of approximately 1-3 mils. If the pad is a circle of diameter (p) then d is preferably less than or equal to r. If the pad is a square of side (l), then d is preferably less than or equal to l/2. This constraint on d permits probe tips (16) to move about laterally without sliding of the pad (16). If the only concern is that a probe tip (16) not slide into an adjacent pad, then d is less than about one half the distance between pads. As the compliant high density probe (10) is pressed against the IC device (30), the probe wire (15) rotates slightly and the probe tip (16) slides along the surface of the bond pads (31) of the IC device (30). The length of the sliding or wiping action is restricted by the angle and length of the probe wire (15) and the amount of compression of the probe (10). The probe (10) mounted on substrate (11) is designed and adapted for being moved by a means for moving probe (10) towards electronic device (30) so that probe tips (16) are moved towards pads (21) on electronic device (30) so that probe tips (16) contact pads (21) sot that probe (10) can be used to electrically test and burn in device (30).

FIGURE 2 shows a magnified cross section of a preferred embodiment of the complaint test probe. The thin sheet (20) can be insulated by conformally coating a thin layer of either an organic or an inorganic material on both surfaces and into the holes (21) in the thin sheet (20). The organic coating, for example, could be Parylene C, Parylene D or Parylene F, or any other types known in the arts. Coating (24) is most desirable if sheet (20) is an electrically conducting material. If sheet (20) is electrically conducting, sheet (20) can be electrically biased, such as being held at ground potential to provide electrical shielding between electrical conductors (15) and between electrically conductive pads (31) to avoid crosstalk between conductors (15) and pads (31).

FIGURE 3 shows a first process used to fabricate the compliant test probe (10). A thermosonic wire bonder tool is used to attach ball bonds (14) to the fan out wiring (13) on the first surface (12) of the substrate (11) which is preferably rigid. The wire bonder tool uses a first, preferably ceramic, capillary (40) to press the ball shaped end (14) of the bond wire (41) against the wiring (13) on the first surface (12) of the substrate (11). Compression force and ultrasonic energy are preferably applied through the first capillary (40) tip and thermal energy is preferably applied from the wire bonder stage through the substrate (11) to bond the ball shaped end (14) of the bond wire (41) to the fan out wiring (13) on the first surface (12) of the substrate (11). The bond wire (41) is positioned at an angle and a shear blade (42) is used to sever the bond wire (41) to create an angled segment of wire (15) protruding away from the ball bond (14) initially vertically away from ball (14). The movement of the capillary (40) is controlled during this process to provide a short straight section of the wire (43) that is preferably perpendicular to the surface of the rigid substrate (11). By controlling the relative movement between capillary (40) and substrate (11) a variety of

shapes of wire (15) can be achieved, such as continuously curved. FIGURE 15 schematically shows examples of shapes.

FIGURE 4 shows (preferably an argon-ion) laser (50) used to melt the ends of the short straight sections of the wire (15) to create a ball shaped contact (16). A thin sheet (20) with holes (21) corresponding to the ends of the probe wires (15) is placed over the array of wires (15) and supported by a preformed frame (17). The thin sheet (20) preferably has a thickness from 1-10 mills. The polymer coating (24) on the thin Invar sheet (20) is applied prior to this process. The preformed frame (17) which is preferably made of a high compliance foamed elastomer material. Alternatively, frame (17) can be a spring. A thin (preferably metal) metal mask (51) with precision located holes (52) corresponding to the ends of the probe wires (15) is placed over the array of wires (15). The mask (51) protects the polymer coating (24) on the thin Invar sheet (20) from the (preferably argon-ion) laser (50) while the ball shaped contacts (16) are being formed on the ends of the probe wires (15). Mask (51) is made of a material which blocks, such as by absorption,the laser from reaching the polymer coating (24). The smooth surface of the ball shaped contact (16) is ideal for a wiping interface. The size of the ball shaped contact (16) on the end of the probe wire (15) is controlled by the laser power density and the alignment of the focal point of the sense focusing the laser beam from the tip of the straight wire section (43). The diameter of the holes (52) in the thin metal mask (51) are preferably slightly larger than the diameter of the ball shaped contacts (16) to allow the mask (51) to be removed after the balls (16) are formed.

The space between the probe wires (15) is preferably filled with an elastomer. FIGURE 5 shows a process used to fill the empty space

between the array of high density probes (15) with a liquid elastomer resin (61). Preferably the preformed elastomer frame (17) supporting the thin Invar sheet (20) acts as a casting dam to contain the liquid elastomer resin (61) until it is cured. A controlled volume (60) of liquid elastomer resin (61) is dispensed into the cavity through a small opening (22) in the thin sheet (20) preferably using a syringe and a small capillary tube. The liquid elastomer resin (61) is forced into the cavity under pressure similar to an injection molding process. The liquid elastomer resin (61) can also be injected into the probe cavity through an opening in the preformed elastomer frame (17). The height of the elastomer resin (61) is controlled by the presence of the thin sheet (20), the ball shaped contacts (16), and the preformed elastomer frame (17). Any excess elastomer resin (61) will be forced out of second small hole (23) in the thin sheet (20). After the cavity is completely filled, the probe assembly is placed in an oven to cure the elastomer resin (61).

FIGURES 1-5 show a method of forming a probe structure for a single IC device. This method can be used to fabricate an array of test probe structures on a single substrate.

FIGURE 6 shows a cross section of a compliant test probe array (100) for testing multiple IC devices on a single wafer. The integrated test probe (100) shown in FIGURE 6 includes four distinct probe arrays used to test individual IC devices on the wafer (130). The construction of each distinct probe array is identical to that shown in FIGURE 1. The substrate (110) used as the base for building the test probe has an array of pads (113) on the top surface (112) that matches the pattern of contacts (131) on the wafer (130) to be tested. The test probes are bonded to these pads (113) and formed at an angle or in an arbitrary shape as described in the

FIGURES 3 to 6 and 15. The angle or shape of the bond wires (115) are preferably the same to ensure accurate positioning of the ball shaped contact (116) on the end of the probe. Uniform material properties and uniform height of the elastomer material (118) are preferable to provide optimum compliance and contact normal force across the entire surface of the probe array. Although FIGURE 6 shows the preformed elastomer frame (117) located between each array of probes, the elastomer frame (117) can be selectively arranged to minimize the spacing between probe arrays.

FIGURE 7 shows a top view of a compliant test probe array (100) for testing all of the IC devices on a single wafer the outline of which is shown as (130). The integrated test probe (100) shown in FIGURE 7 includes twelve distinct probe arrays used to test all of the IC devices on the wafer (130). The outline of the wafer (130) and the individual IC devices (133) are shown with broken or dashed lines. The location of each array of probes corresponds with the pads on each of the individual IC devices (133) on the wafer (130). The location of the ball shaped ends (116) of the test probes is accurately controlled by the location of the openings in the thin sheet (120).

FIGURE 8 shows a cross section of another embodiment of a compliant test probe. The first alternate embodiment uses a thin sheet (20) similar to the embodiment of FIGURES 1-6 without the polymer coating and the diameter of the holes (21) in the {preferably of electrically conductive, such as Invar sheet (20)} are slightly larger. A thin polymer sheet (25) with smaller diameter holes (26) is laminated over the thin sheet (20). The thin polymer sheet can be polyimide, mylar and polyethylene. This list is exemplary only and not limiting. The smaller diameter holes (26) are slightly larger than the probe wire (15) diameter and are used to provide accurate alignment of the

probe contacts (16). The smaller diameter holes (26) also prevent the probe wires (15) from making contact with the sides of the holes (21) in the conductive sheet (20). The thin polymer sheet (25) is preferably segmented and bonded to the thin sheet (20) to eliminate TCE mismatch problems over large surface areas. A second thin polymer sheet could be laminated or spin-coated on the bottom side of the thin sheet (20), opposite to the first thin polymer sheet (25), to avoid possible bowing problems. FIGURE 9 shows a magnified section of the embodiment of FIGURE 8 with the larger holes (21) in the thin Invar sheet (20) and the smaller holes (26) in the thin polymer sheet (25).

FIGURE 10 shows a cross section of another embodiment of the compliant test probe which uses a thin polymer sheet (25) with small holes (26) to control the location of the probe wires (15). The thin polymer sheet (25) is attached to a thin (preferably rigid, such as Invar) frame (27) that surrounds each array or cluster of probes. The thin polymer sheet (25) is preferably segmented and bonded to the thin frame (27) to eliminate TCE mismatch problems over large surface areas.

FIGURE 11 shows a cross section of another embodiment of the compliant test probe which uses a thin (preferably Invar) sheet (20) with a thin polymer coating (24) and small diameter holes (21) to control the location of the probe wires (15). The sheet (20) is attached to a thick (preferably Invar) frame (28). The thickness of the frame (28) can be modified to control the total compliance of the test probes (10).

FIGURE 12 shows a cross section of another embodiment of the compliant test probe. The forth alternate embodiment is identical to the preferred embodiment with the exception of the elastomer material surrounding the

individual probe wires (15). The compliant test probes (10) are supported by the thin (preferably Invar) sheet (20) and the preformed elastomer frame (17).

FIGURES 13 and 14 show a cross section and top view of another embodiment of the compliant test probe array for testing multiple IC devices on a single wafer. The configuration of probes in this embodiment is typical of memory devices having two rows of contacts per device. Each array of probes is decoupled from the adjacent arrays by slots (125) in the thin (preferably Invar) sheet (120).

FIGURE 15 schematically shares a variety of shapes of probe wires useful to practice the present invention, such as "S" showed "C" shaped, continuously curved, piece wire curved, piece wire linear and combinations thereof.

FIGURE 16 schematically shows alternative embodiments of compliant frame structures (17) to support probe tip positioning structure (20) to be maintaining in position and to move as the probe tip ends (16) move when they are moved into engagement with electronic device pads (31).

FIGURE 17 shows examples of elongated electrical conductors (202) having a coating (204) disposed thereon. Preferably coating (204) is at the surface of elongated conductor (202) leaving the end of conductor (202) exposed. Hard coating 204 can provide a reinforcing hard coat. Coating 204 is preferably a hard metal such as Pd, Pt, Ni, Au, Rh, Ru, Re, Cu, Co and their alloys, etc. Elongated conductor 206 has a protuberance 208 at the distal end having such a hard coating 210. Elongated conductor 212 has an end 214 with sharp spikes 216, preferably on the surface 218 of

protuberance 220.

FIGURE 18 schematically shows an apparatus for moving probe structure 10 towards and away from electronic device 204 so that probe tips 210 engage and disengage electrical contact locations 212 on electronic device 204. Probe 10 is mounted on to holder 200 having means 214 for applying electric power to the probe tips 210. Electronic device 206 is held on base 206. Holder 200 is physically connected to support 202 which is converted to arm 208 which is converted to base 206. Support 202 is adapted for up and down movement. Examples of an apparatus to provide the means for support and up and down movement can be found in US Patent 5,439,161 and U.S. Patent 5,132,613, the teachings of which are incorporated herein by reference.

While we have described our preferred embodiments of our invention, it will be understood that those skilled in the art, both now and in the future, may make various improvements and enhancements which fall within the scope of the claims which follow. All references cited in this application herein are incorporated by reference herein.

The teaching of the following patent co-pending applications are incorporated herein by reference:

U.S. Patent 5,371,654 entitled, "THREE DIMENSIONAL HIGH PERFORMANCE INTERCONNECTION PACKAGE";

U.S. Patent Application Serial No. 08/614,417 entitled, "HIGH DENSITY CANTILEVERED PROBE FOR ELECTRONIC DEVICES";

U.S. Patent Application Serial No. 08/641,667 entitled, "HIGH DENSITY TEST PROBE WITH RIGID SURFACE STRUCTURE";

U.S. Patent Application Serial No. 08/527,733 entitled, "INTERCONNECTOR WITH CONTACT PADS HAVING ENHANCED DURABILITY";

U.S. Patent Application Serial No. 08/752,469 entitled, "FOAMED ELASTOMERS FOR WAFER PROBING APPLICATIONS AND INTERPOSER CONNECTORS";

U.S. Patent Application Serial No. 08/744,903 entitled, "INTEGRAL RIGID CHIP TEST PROBE";

U.S. Patent Application Serial No. 08/756,831 entitled, "HIGH TEMPERATURE CHIP TEST PROBE";

U.S. Patent Application Serial No. 08/756,830 entitled, "A HIGH DENSITY INTEGRAL TEST PROBE AND FABRICATION METHOD";

U.S. Patent Application Serial No. 08/754,869 entitled, "HIGH DENSITY INTEGRATED CIRCUIT APPARATUS, TEST PROBE AND METHODS OF USE THEREOF".

It is to be understood that the above described embodiments are simply illustrative of the principles of the invention. Various other modifications and changes may be devices by those of skill in the art which will embody the principles of the invention and fall within the spirit and scope thereof.

CLAIMS

What is claimed is:

1. A structure comprising:

a substrate having a surface;

a plurality of elongated electrical conductors extending away from said surface;

each of said elongated electrical conductors having a first end affixed to said surface and a second end projecting away from said surface;

there being a plurality of said second ends;

a means for maintaining said plurality of said second ends in substantially fixed positions.

2. A structure according to claim 1 wherein said first end is affixed to said surface at an electrical contact location.

3. A structure according to claim 1 wherein said means for maintaining is a sheet of material having a plurality of opening therein through which said second ends project.

4. A structure according to claim 1 wherein at said second end there is

disposed a structure selected from the group consisting of a protuberance and a sharp spike.

5. A structure according to claim 3 wherein said sheet is formed from a material selected from the group consisting of a rigid material and a compliant material.

6. A structure according to claim 3 wherein said sheet comprises a sheet of electrically conductive material having a plurality of through holes therein, said sheet of material contains a dielectric material to provide a means for preventing said elongated electrical conductors from electrically contacting said sheet of electrically conductive material.

7. A structure according to claim 3 wherein said sheet is spaced apart from said surface by a flexible support.

8. A structure according to claim 7 wherein said flexible support is selected from the group consisting of a spring and an elastomeric material.

9. A structure according to claim 1 wherein said elongated electrical conductors have a shape selected from the group consisting of linear, piece wise linear, curved and combinations thereof.

10. A structure according to claim 7 wherein said sheet and said flexible support form a space containing said plurality of elongated electrical conductors.

11. A structure according to claim 10 wherein said space is filled with a

flexible material.

12. A structure according to claim 11 wherein said flexible material is an elastomeric material.

13. A structure according to claim 6 wherein said sheet has a top surface and a bottom surface and said through holes have a sidewall, said dielectric material coats said top surface and said bottom surface and said sidewall.

14. A structure according to claim 1 wherein said plurality of elongated electrical conductors are distributed into a plurality of groups.

15. A structure according to claim 14 wherein said plurality of groups are arranged in a array.

16. A structure according to claim 1 wherein said structure is a probe for an electronic device.

17. A structure according to claim 16 wherein said electronic device is selected from the group consisting of an integrated circuit chip and a packaging substrate.

18. A structure according to claim 15 wherein each of said groups corresponds to an integrated circuit chip on a substrate containing a plurality of said integrated circuit chips.

19. A structure according to claim 18 wherein said substrate containing said plurality of integrated circuit chips is a wafer of said integrated circuits

chips.

20. An apparatus for using said structure of claim 1 to test an electronic device comprising:
means for holding said structure of claim 1, means for retractably moving said structure of claim 1 towards and away form said electronic device so that said second ends contact electrical contact locations on said electronic device, and means for applying electrical signals to said elongated electrical conductors.

21. A structure according to claim 4 wherein said protuberance is spherelike.

22. A structure according to 3 wherein said sheet comprises a sheet of electrically conductive material having a plurality of first through holes therein, and a sheet of a dielectric material having a plurality of second through holes therein, said first through holes are aligned with said second through holes, said first through holes have a smaller diameter than said second through holes to provide a means for preventing said elongated electrical conductors from electrically contacting said sheet of electrically conductive material.

23. A structure according to claim 22 wherein sheet or electrically conductive material has a first side and a second side, said sheet of dielectric material is disposed on either of said first side and said second side of said sheet of electrically conductive material.

24. A structure according to claim 23, where there is disposed on said first side and said second side of said sheet of electrically conductive

material a layer of said dielectric material.

25. A structure according to claim 3 wherein said sheet comprises a sheet of rigid material having a plurality of through holes therein, said sheet contains a dielectric material to provide a means for preventing said elongated electrical conductors from electrically contacting said sheet of electrically conductive material.

26. A structure according to claim 3 wherein said sheet comprises a sheet of dielectric material having a plurality of through holes therein, said sheet contains a sheet of a rigid material disposed in contact with said sheet of dielectric material, said sheet of rigid material has on opening therein exposing a plurality or said through holes to provide a means for support of said dielectric material.

27. A structure according to claim 26 wherein said sheet is spaced apart from said surface by a flexible support, said sheet of rigid material is disposed on said flexible support.

28. An apparatus for making electrical contact with a plurality of bond pads on an integrated circuit device comprising:
a first fan out substrate having a first surface;
said first surface having a plurality of contact locations;
a plurality of ball bonds attached to said plurality of contact locations;
a plurality of wires extending outward from said ball bonds, away from said first surface on fan out substrate;
a plurality of ball shaped contacts on the ends of said plurality of wires; and
a means for maintaining said plurality of balls in substantially fixed

positions.

29. A high density probe according to claim 28, wherein said fan out substrate is selected from the group consisting of:
multilayer ceramic substrates with thick film wiring;
multilayer ceramic substrates with thin film wiring;
metallized ceramic substrates with thin film wiring;
epoxy glass laminate substrates with copper wiring; and
silicon substrates with thin film wiring.

30. A high density probe according to claim 28, further including a preformed frame of foamed elastomer material surrounding clusters, groupings, or arrays of said probes.

31. A high density probe according to claim 30, further including a layer of elastomer material surrounding said probes in said cluster.

32. A high density probe according to claim 31, wherein said means for maintaining is a sheet of Invar material that has a thin coating of a polymer material and a plurality of openings corresponding to said plurality of ball shaped contacts.

33. A high density probe according to claim 31, further including a sheet of rigid material with a plurality of large diameter openings corresponding to said plurality of ball shaped contacts.

34. A high density probe according to claim 33, further including a sheet of polymer material with a plurality of small diameter openings

corresponding to said plurality of ball shaped contacts place on top of said sheet of Invar material.

35. A high density probe according to claim 37, further including a sheet of polymer material with a plurality of openings corresponding to said plurality of ball shaped contacts.

36. A high density probe according to claim 35, further including a frame of rigid material attached to said sheet of polymer material with said plurality of openings corresponding to said plurality of ball shaped contacts.

37. A high density probe according to claim 32, further including a thick frame of rigid material attached to said sheet of Invar material with said thin coating of a polymer material and said plurality of openings corresponding to said plurality of ball shaped contacts.

38. A high density probe according to claim 33, further including a plurality of probes arrays corresponding to the location of a plurality of IC devices on a wafer.

39. A high density probe according to claim 30, further including a sheet of rigid material that has a thin coating of a polymer material and a plurality of openings corresponding to said plurality of ball shaped contacts.

40. A structure according to claim 1 wherein said substantially fixed positions substantially correspond to electrical contact locations on a device to be tested by said probe.

41. A method comprising:

providing a substrate having a surface;

forming a plurality of elongated electrical conductors extending away from said surface;

each of said elongated electrical conductors having a first end affixed to said surface and a second end projecting away from said surface;

there being a plurality of said second ends;

providing a means for maintaining said plurality of said second ends in substantially fixed positions with respect to each other.

42. A structure according to claim 3 wherein said sheet is formed and material selected from the group consisting of Invar, Cu/Invar/Cu, molybdenum, polyimides.

43. A structure according to claim 3 wherein said sheet is formed from a material selected from the group consisting of a metal, a polymer, a semiconductor and dielectric.

44. A structure according to claim 43 wherein said dielectric is selected from the group consisting of a ceramic and a glass.

45. A structure according to claim 1 where at least a part of said elongated

conductor is coated with a hard coat.

46. A structure according to claim 45 wherein said hard coat is selected from the group consisting of Pd, Pt, Ni, Au, Rh, Ru, Re, Cu, Co alloys thereof and combinations thereof.

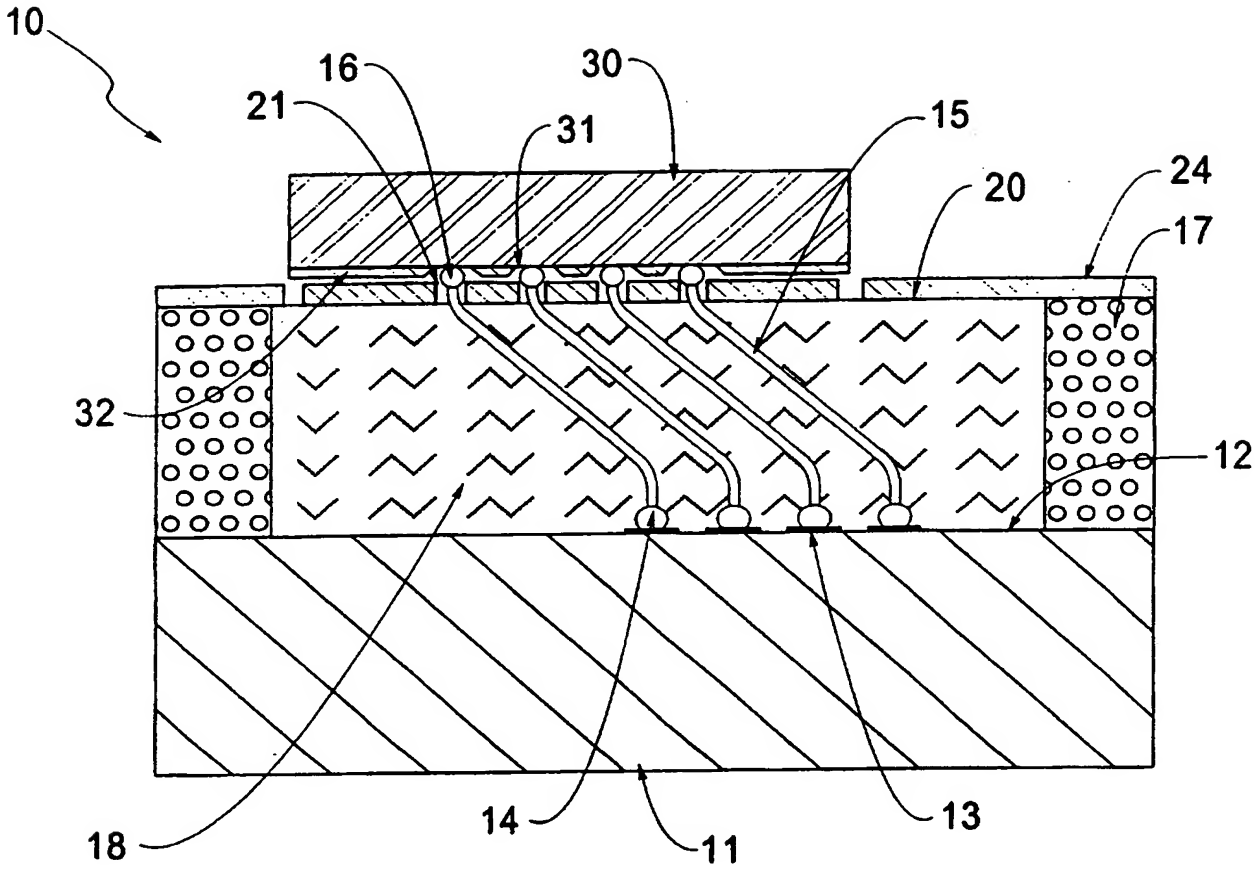

Fig. 1

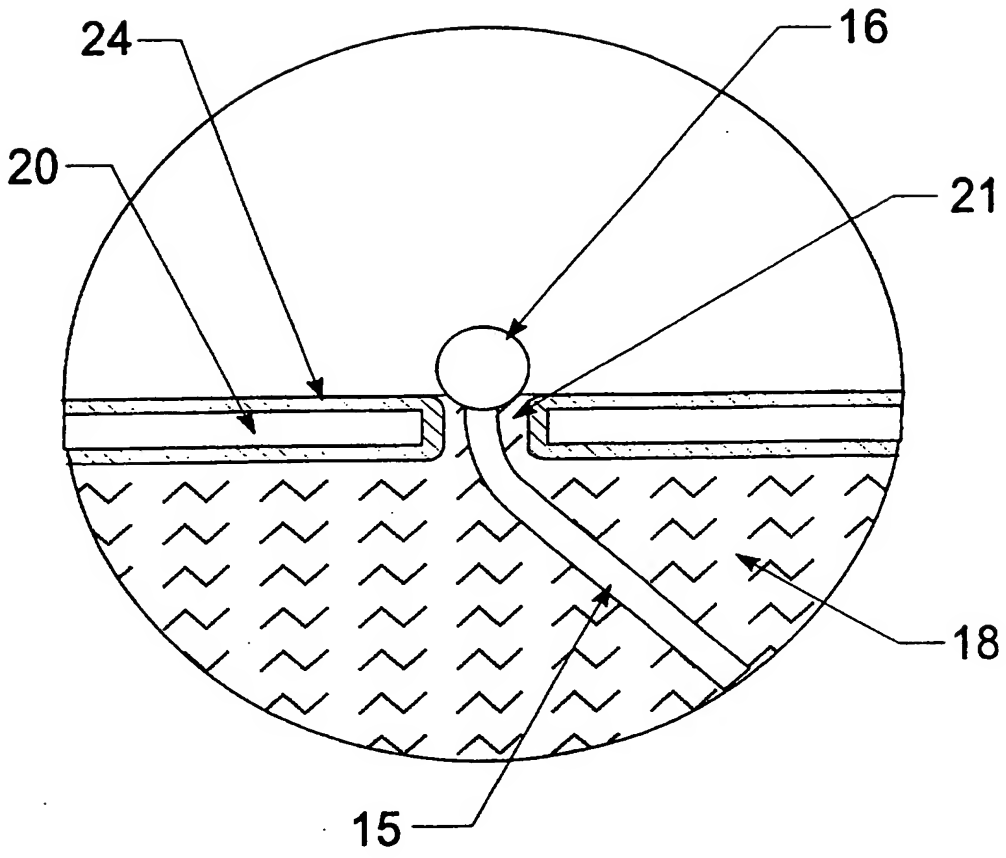

Fig. 2

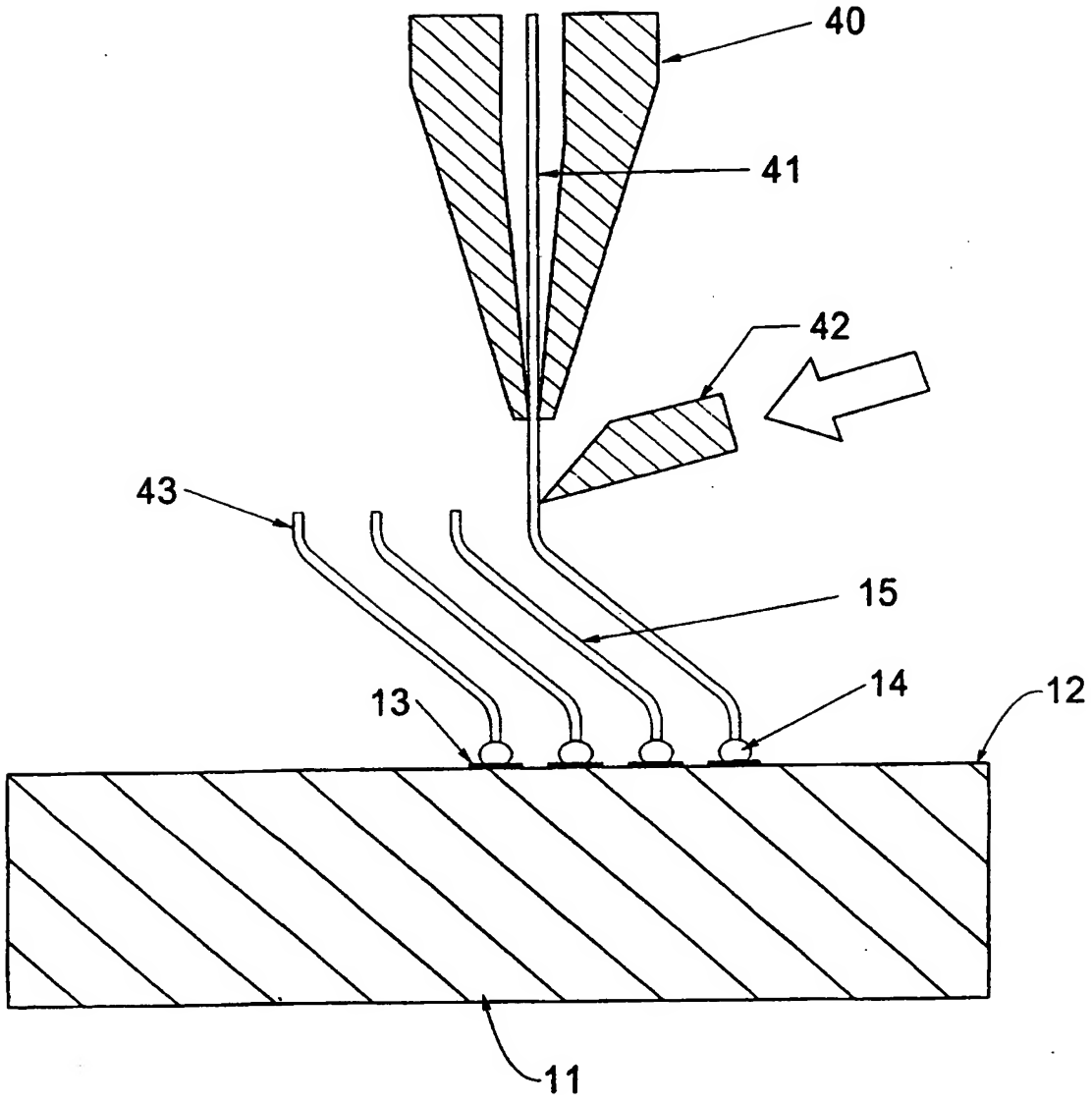

Fig. 3

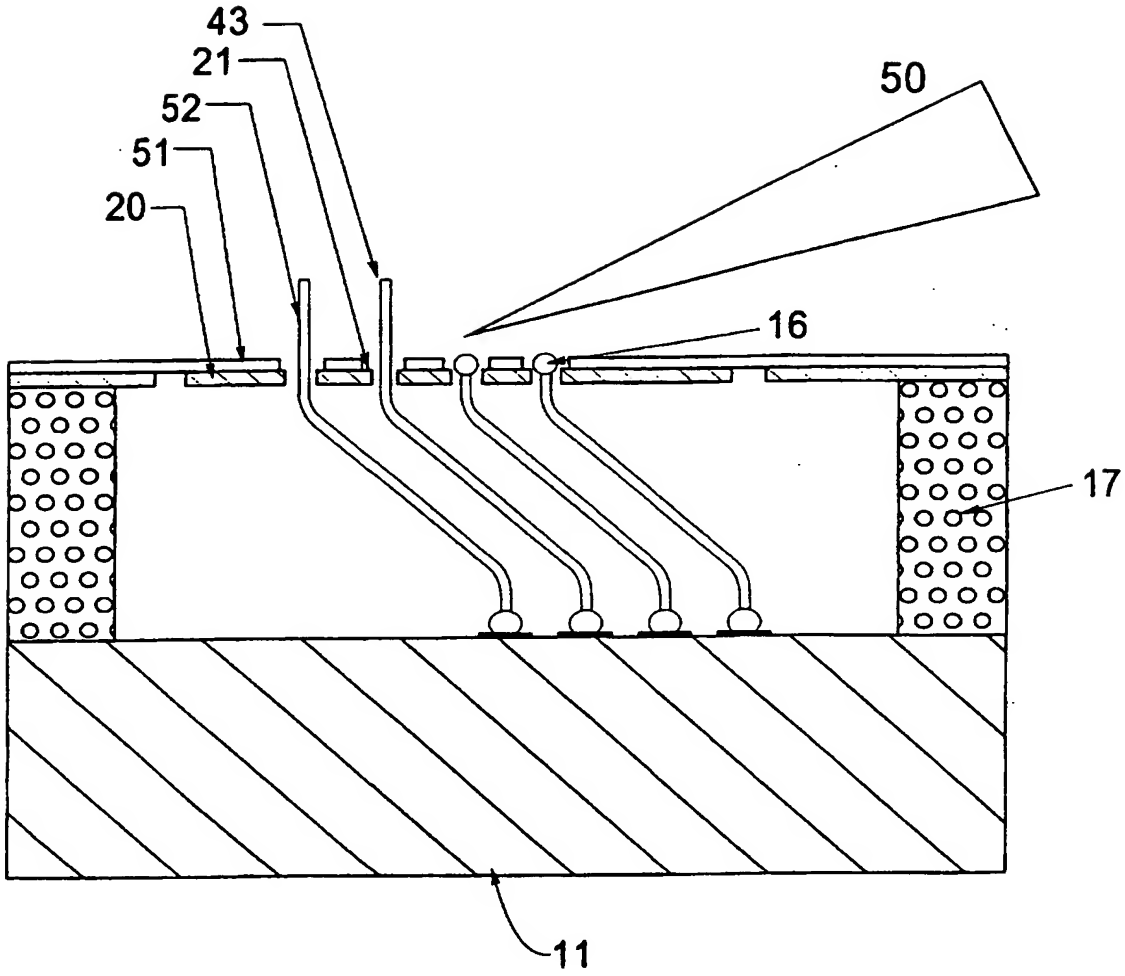

Fig. 4

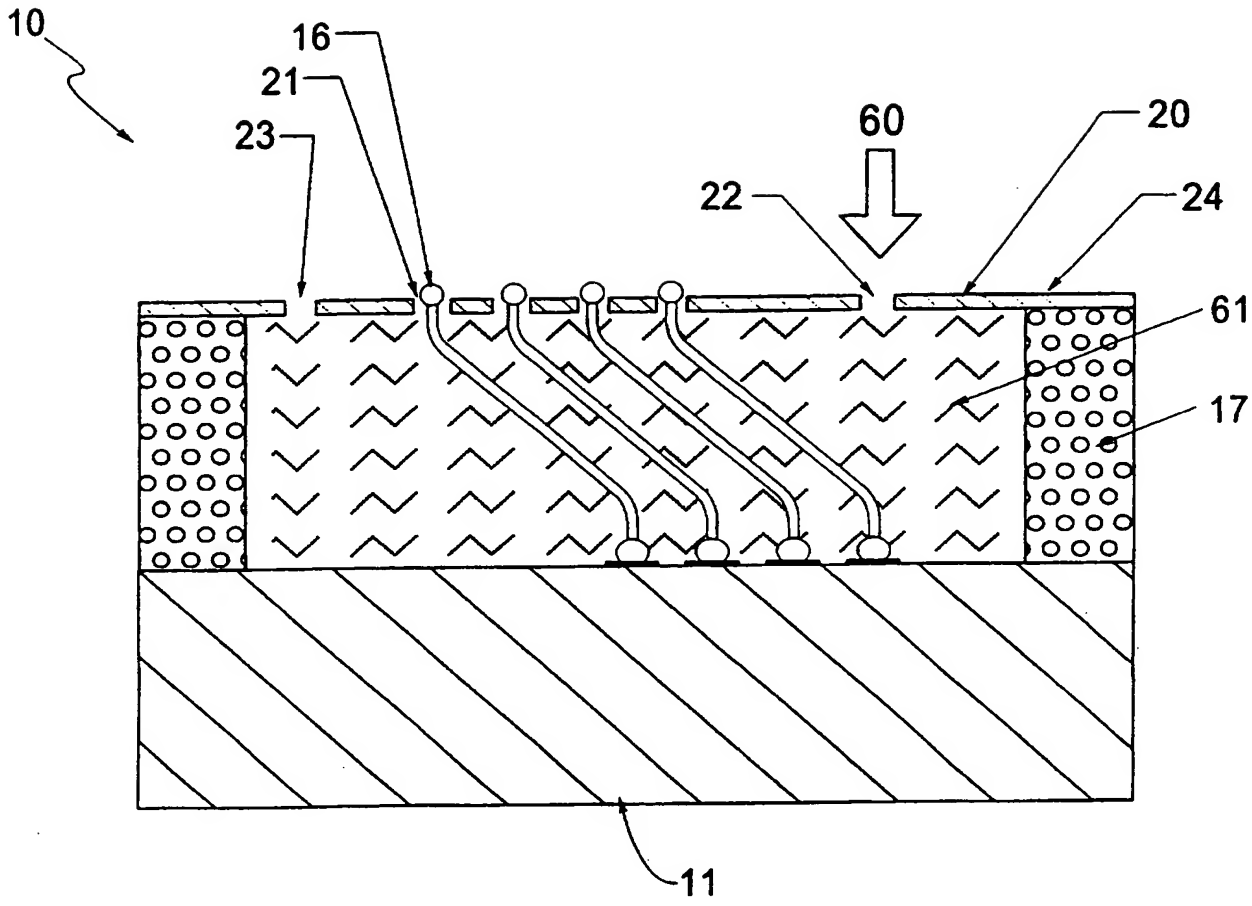

Fig. 5

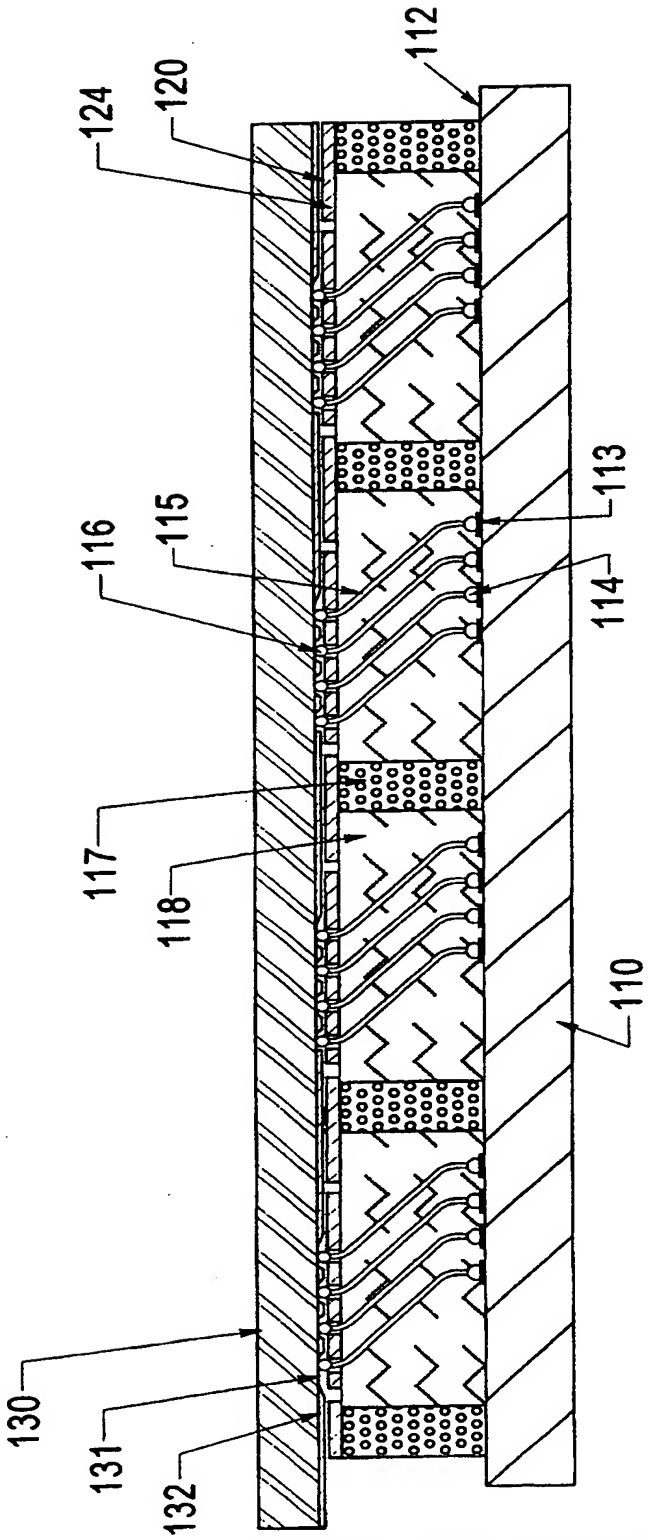

Fig. 6

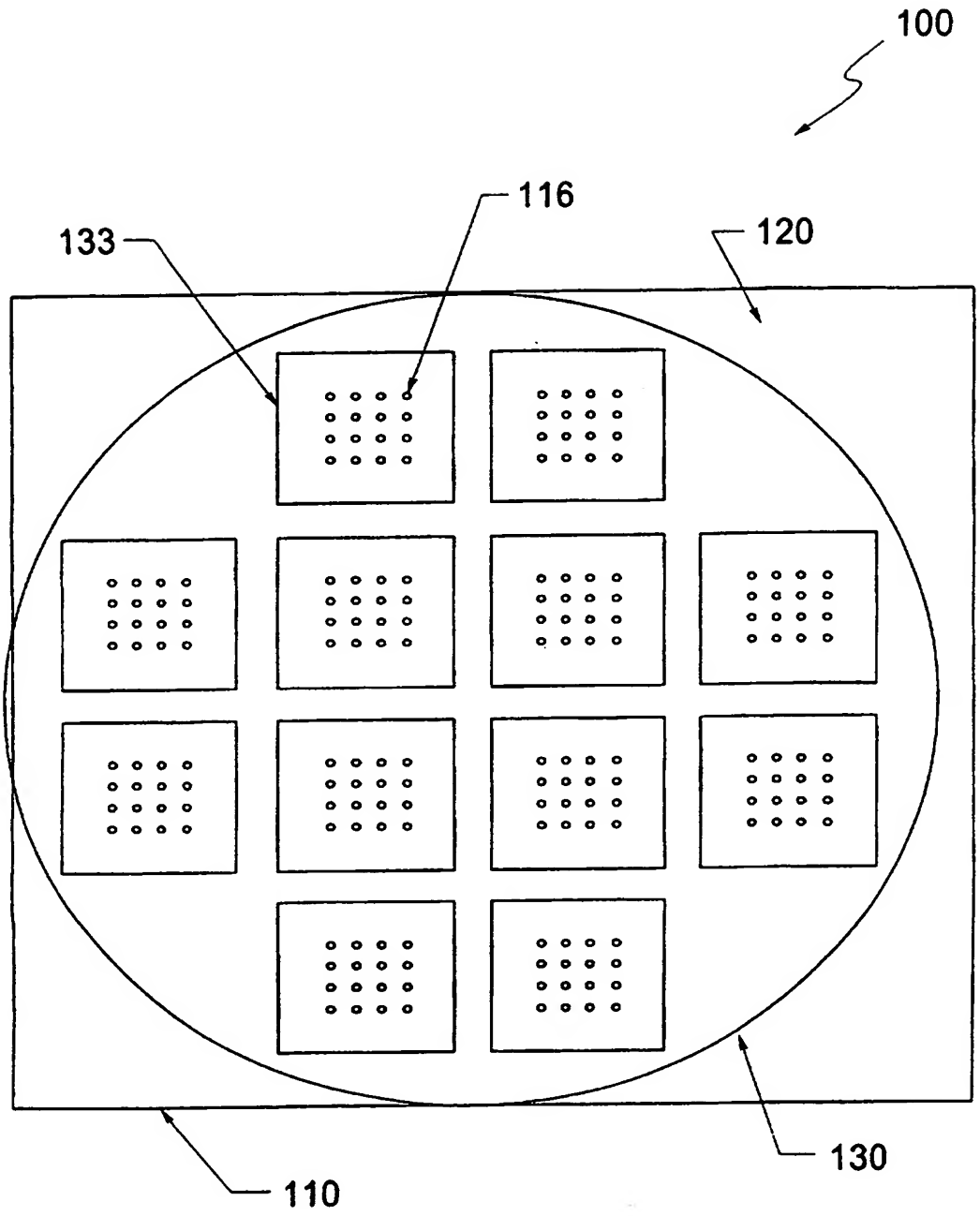

Fig. 7

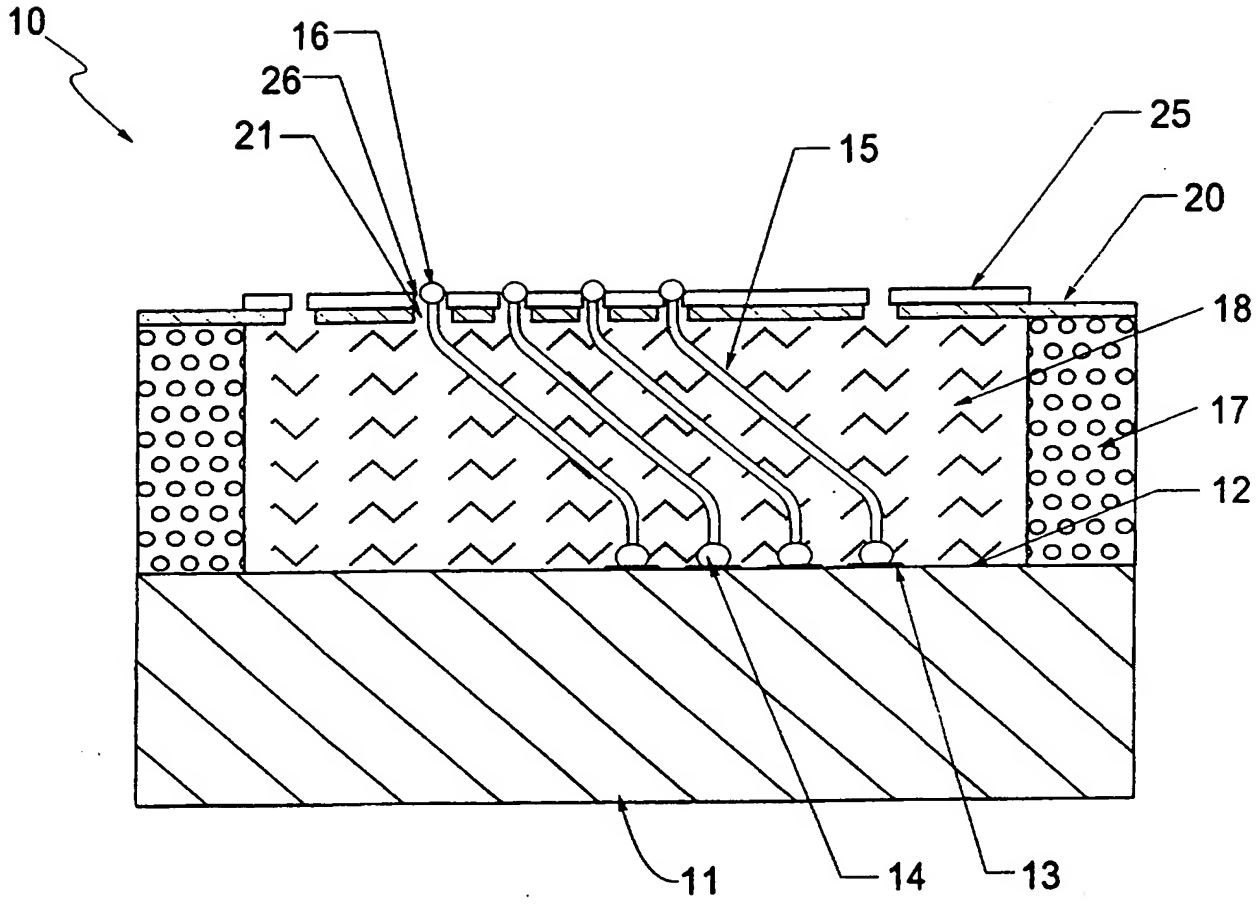

Fig. 8

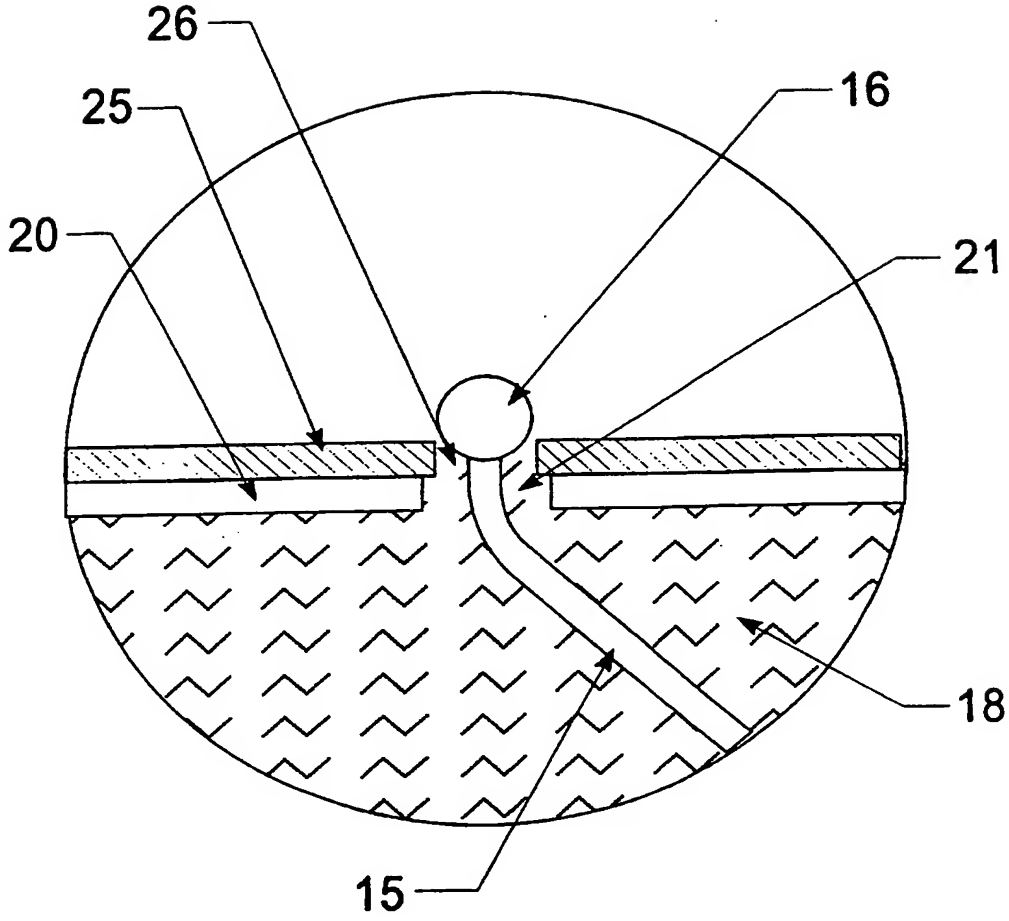

Fig. 9

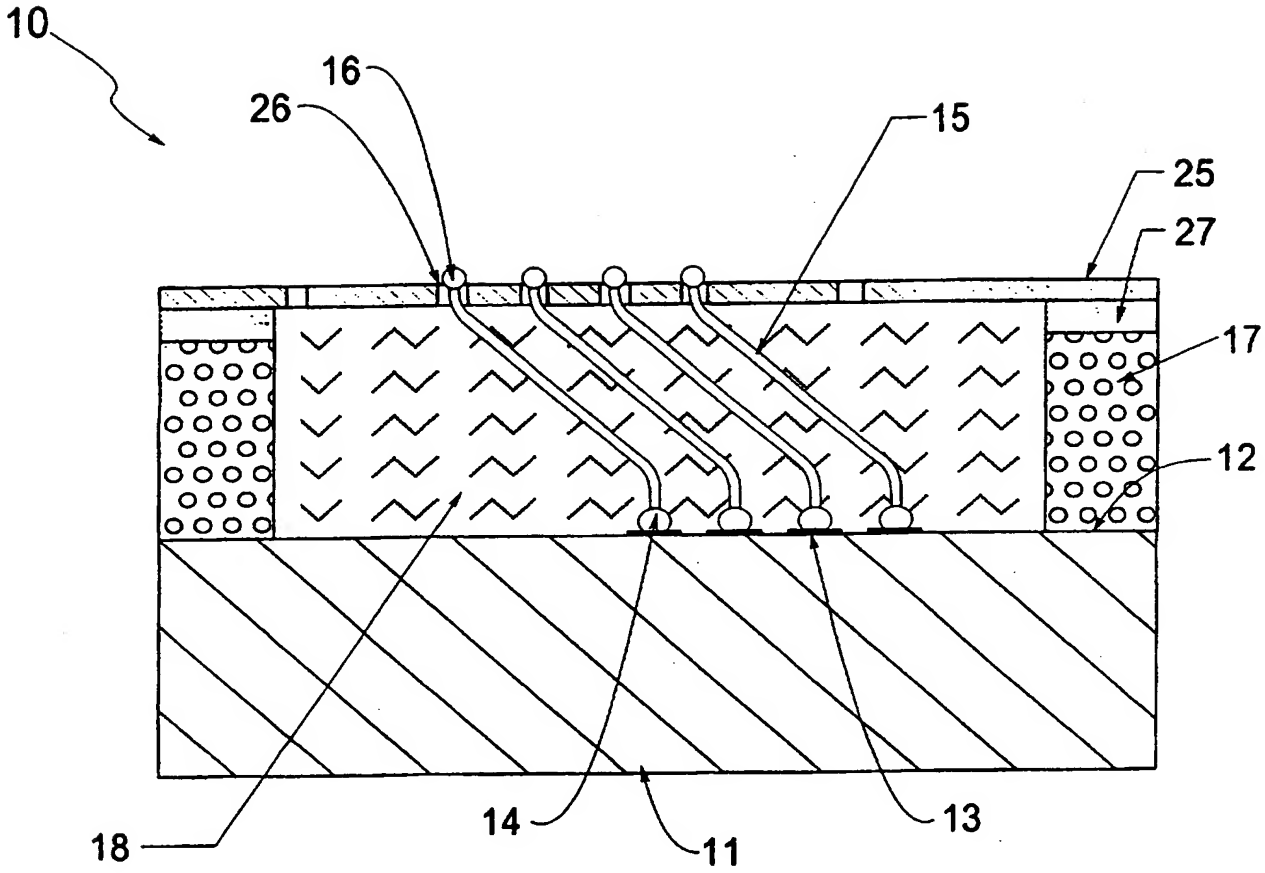

Fig. 10

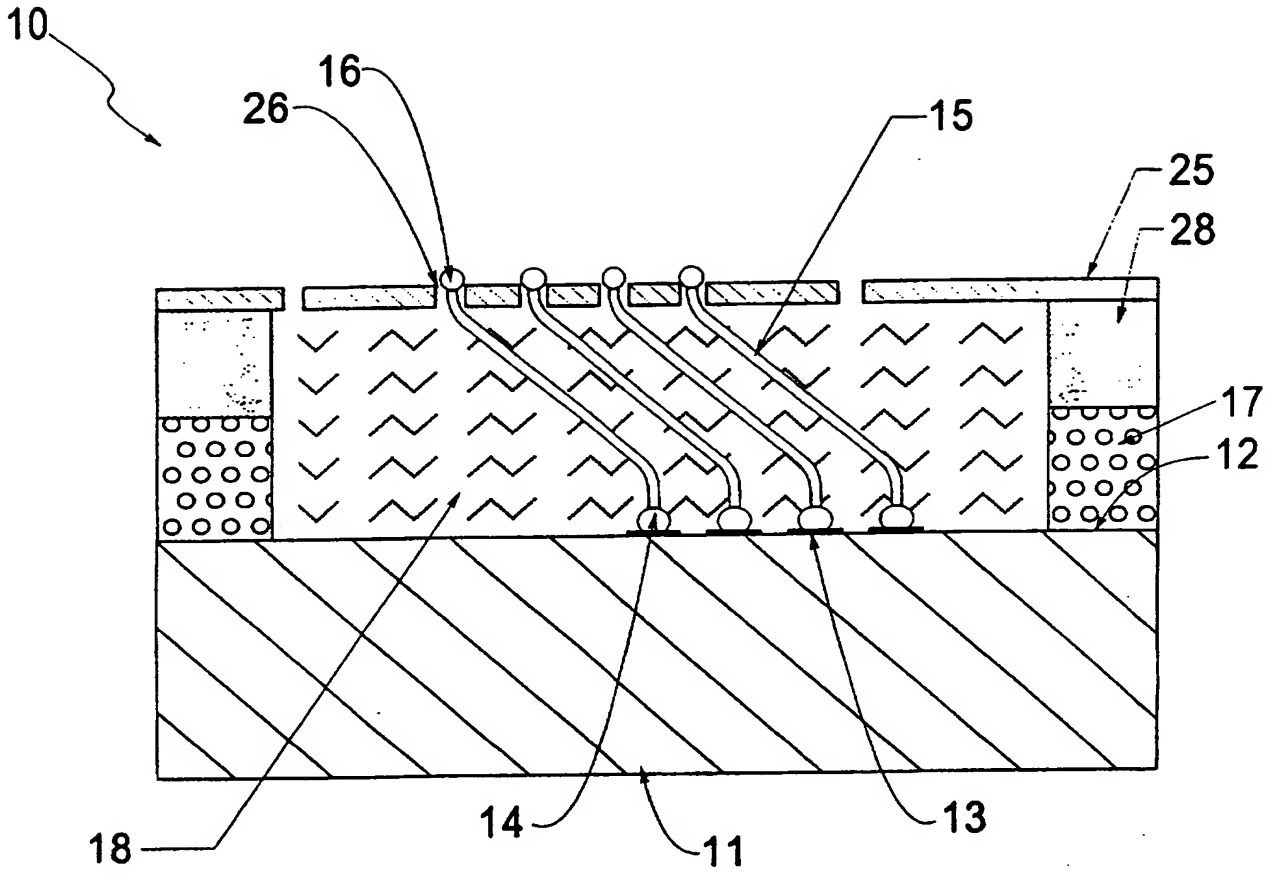

Fig. 11

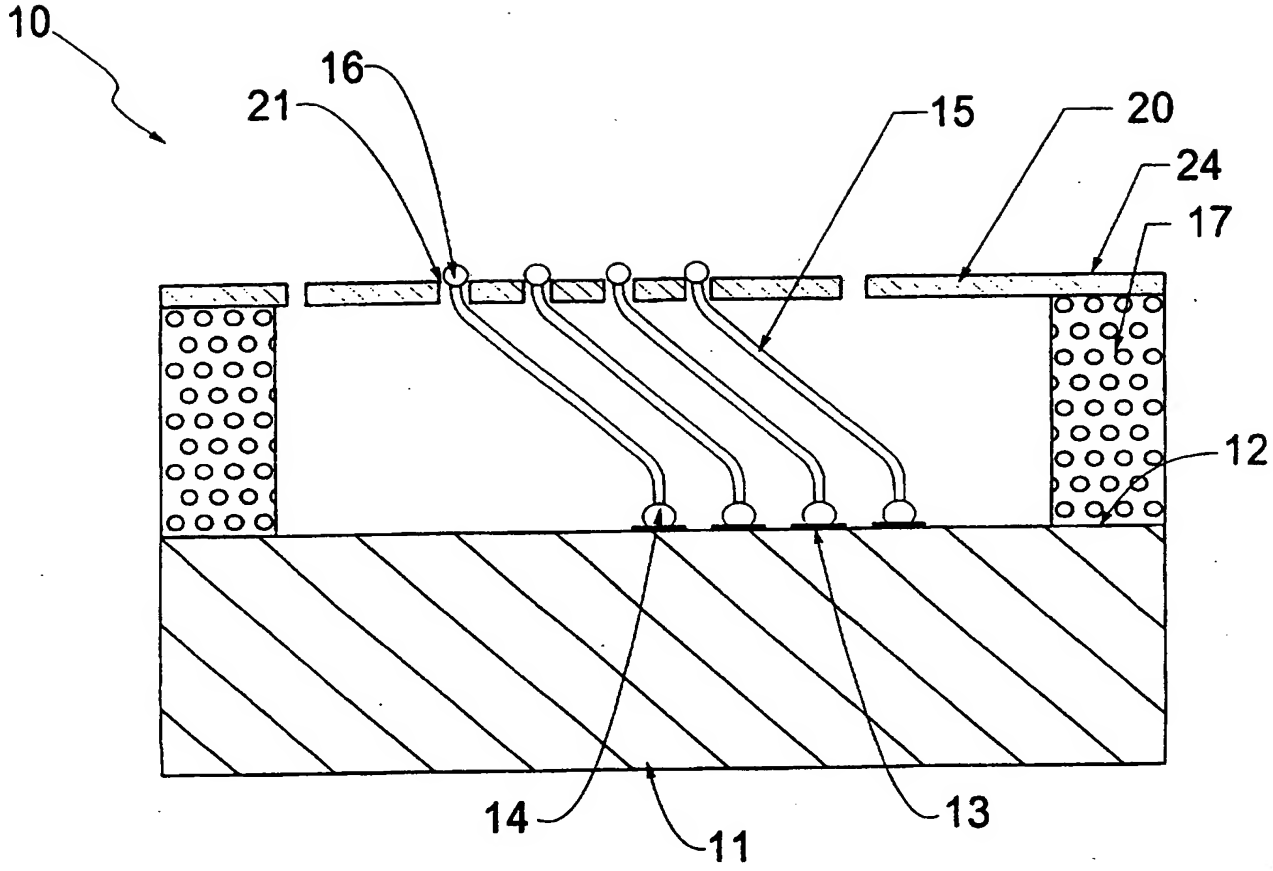

Fig. 12

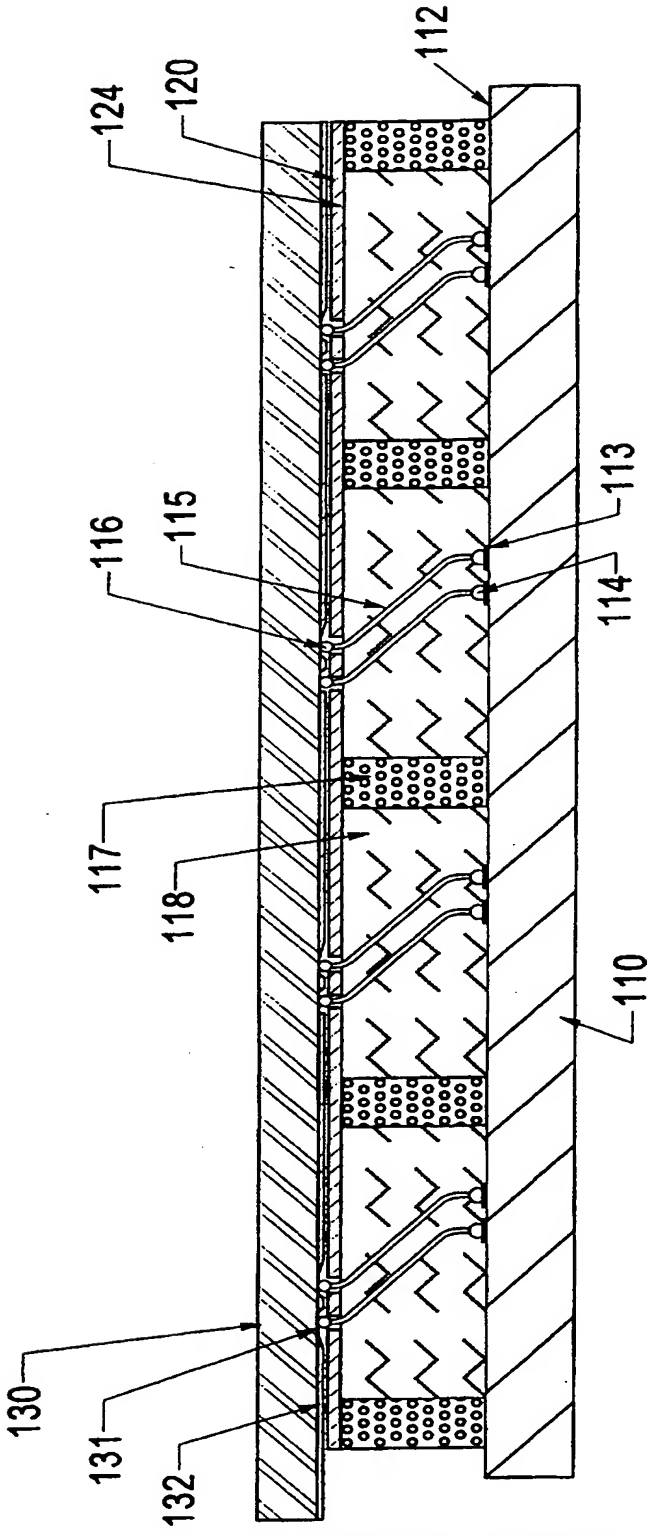

Fig. 13

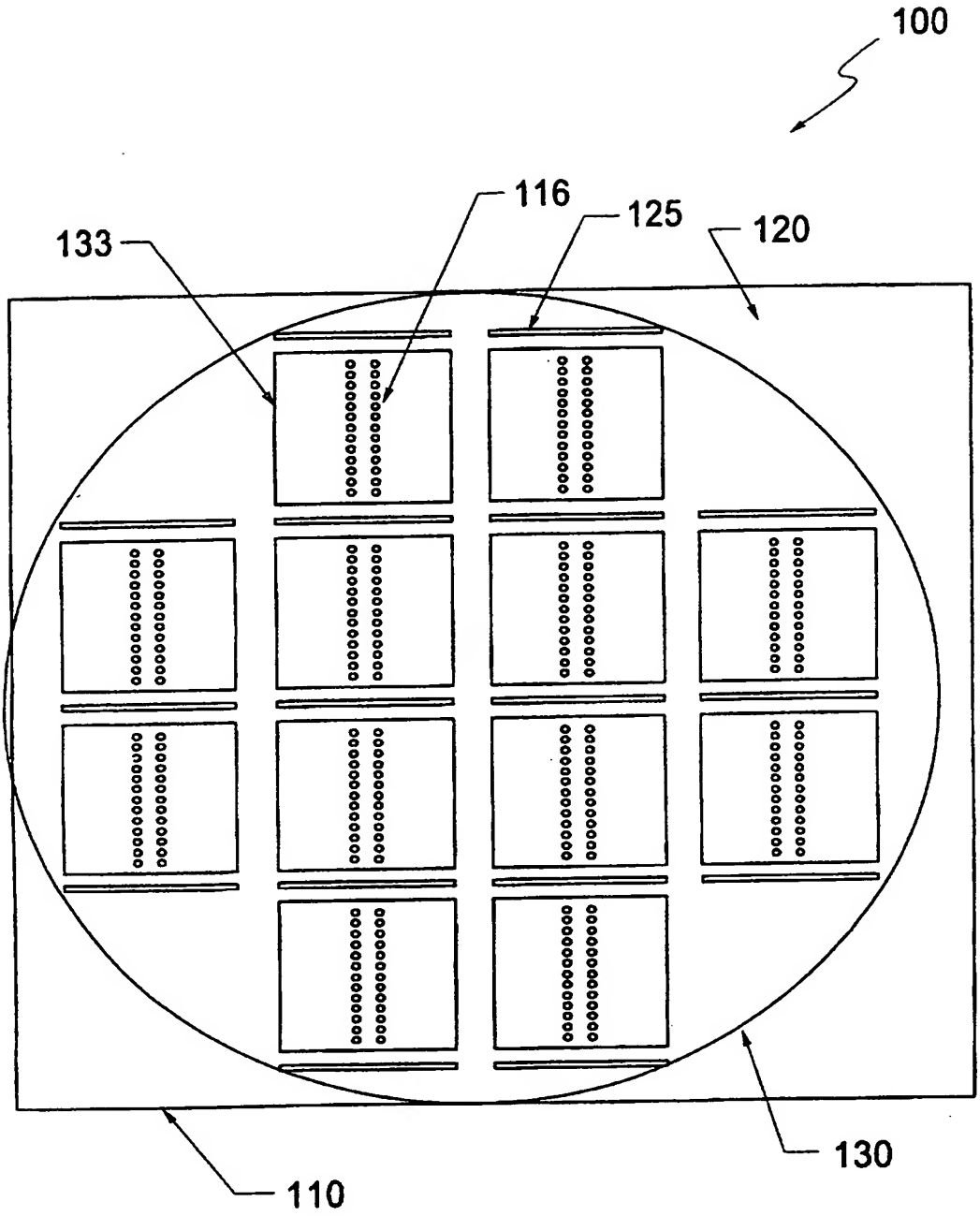

Fig. 14

Fig.15

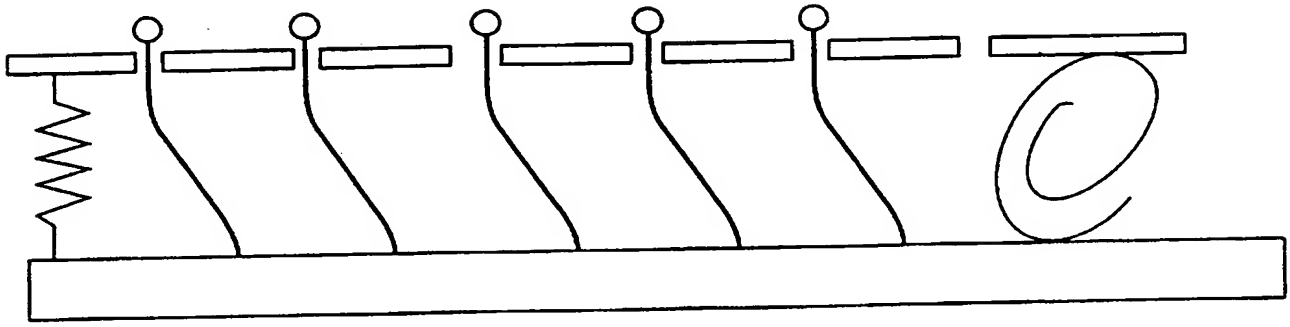

Fig. 16

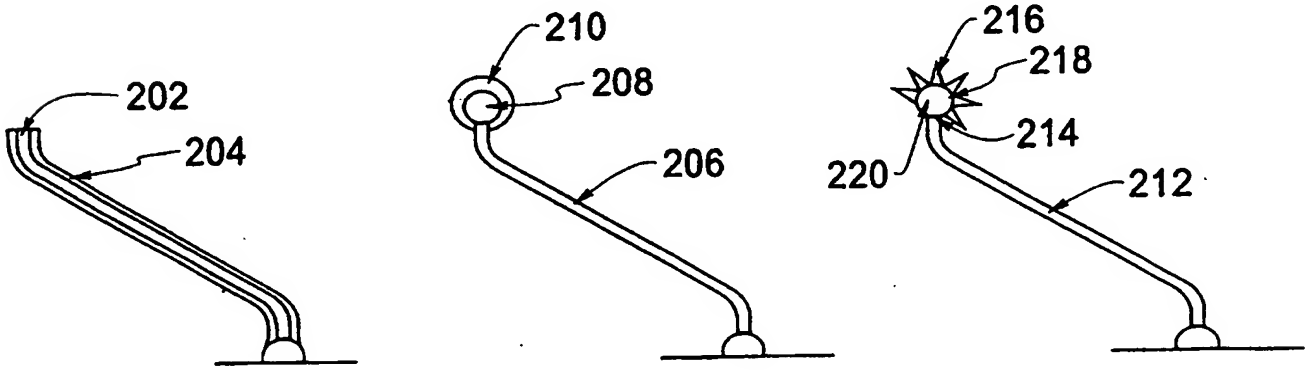

Fig. 17

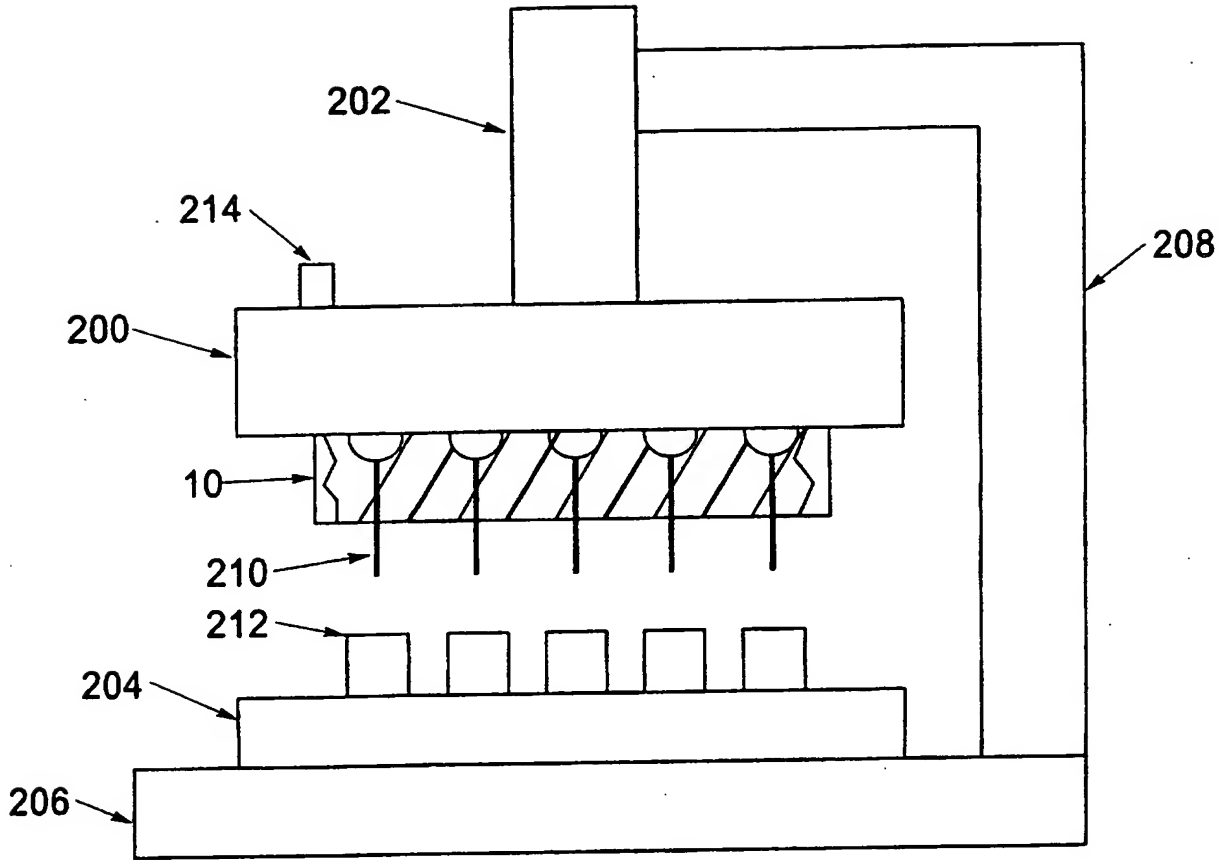

Fig. 18

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 97/16265

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G01R1/073

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	SHIH D -Y ET AL: "A NOVEL ELASTOMERIC CONNECTOR FOR PACKAGING INTERCONNECTIONS, TESTING AND BURN-IN APPLICATIONS" PROCEEDINGS OF THE ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE, LAS VEGAS, MAY 21 - 24, 1995, no. CONF. 45, 21 May 1995, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 126-133, XP000624964	1,2,4,9, 14-19, 21,28, 40,41
Y	see page 131, right-hand column, paragraph 1 - page 133, left-hand column, paragraph 3; figures 1,2,10,13	20,45,46
Y	US 5 266 895 A (YAMASHITA) 30 November 1993 see column 1, line 33 - line 45 see column 4, line 15 - line 64; figures 5A,5B,6A,6B	20

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 December 1997	05/01/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Iwansson, K

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 97/16265

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	ASAI S ET AL: "PROBE CARD WITH PROBE PINS GROWN BY THE VAPOR-LIQUID-SOLID (VLS) METHOD" IEEE TRANSACTIONS ON COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY: PART A, vol. 19, no. 2, 1 June 1996, pages 258-267, XP000594755 see figure 8	45,46
X	PATENT ABSTRACTS OF JAPAN vol. 8, no. 1 (P-246) '1438! , 6 January 1984 & JP 58 165056 A (NIHON DENSHI ZAIRIYOU), 30 September 1983,	1,2,9, 16,17, 40,41
A	see abstract	4,20,21, 28,45,46
X	"HIGH DENSITY PROBE ASSEMBLY" RESEARCH DISCLOSURE, no. 333, 1 January 1992, page 82 (COMPL) XP000281295	1,2,9, 16-19,41
A	see the whole document	10-12
A	ANESI ET AL.: "MULTIPROBE CONTACTOR UNIT" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 14, no. 9, February 1972, NEW YORK US, page 2836 XP002049665 see the whole document	3,5,43

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter...tional Application No
PCT/US 97/16265

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US 5266895 A	30-11-93	JP 5041425 A	19-02-93
		US 5378971 A	03-01-95
		US 5325052 A	28-06-94